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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/611,862

07/03/2003

Tomio Iwasaki

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09/24/2004

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EXAMINER

SMOOT, STEPHEN W

ART UNIT

PAPER NUMBER

2813

DATE MAILED: 09/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/611,862	Applicant(s) IWASAKI ET AL.	
	Examiner Stephen W. Smoot	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 June 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 13-24 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 13,16,19 and 22 is/are rejected.
- 7) ☒ Claim(s) 14,15,17,18,20,21,23 and 24 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 03 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☒ Certified copies of the priority documents have been received in Application No. 09/787,528.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

This Office action is in response to applicant's amendment filed on 09 June 2004. Applicant's submission of a substitute specification on 12 July 2004 is acknowledged and this substitute specification has been entered.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 13, 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schacham-Diamand et al. (US 5,824,599) in view of Bronner et al. (US 5,792,703).

Referring to Fig. 7, Schacham-Diamand et al. disclose a copper plug (23) that is adjacent to a catalytic seed layer (18) that can be platinum or rhodium (also see column 6, lines 13-18, 45-56 and column 7, lines 29-35). Referring to Fig. 13, Schacham-Diamand et al. disclose copper lines (33) that are adjacent to catalytic seed layers (18a) that can be platinum or rhodium (also see column 9, lines 12-40). Schacham-Diamand

et al. further disclose that the catalytic seed layers can be used to line copper-filled contact openings for connecting to doped contact regions (i.e. a diffusion region) (see column 10, lines 54-63). These are limitation set forth in claims 13, 16 of the applicant's invention.

However, although Schacham-Diamand et al. suggest forming the contact between the diffusion region and an overlying copper line, they do not expressly teach or suggest that the diffusion region has a corresponding gate electrode, which is a limitation of claims 13, 16.

Bronner et al. teach a diffusion region (75) formed in a silicon substrate (50) that is adjacent to a gate stack (65) with a metal contact (90) formed through an insulator (85) to electrically connect the diffusion region (75) to an overlying metal line (100) (see Fig. 3 and column 3, line 7 to column 4, line 56). The metal can be a copper alloy (see column 4, lines 46-48).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Schacham-Diamand et al. and Bronner et al. in order to form a copper connection to a diffusion region that corresponds to a gate stack as taught by Bronner et al. Bronner et al. recognize that gate stacks when combined with adjacent diffusion regions can be used to construct field effect transistors (see column 3, lines 7-12).

3. Claims 19, 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bronner et al. (US 5,792,703) in view of Psaras et al. (US 4,803,539).

Referring to Fig. 3 and column 3, line 7 to column 4, line 56, Bronner et al. teach a diffusion region (70) formed in a silicon substrate (50) that is adjacent to a gate stack (60) with a metal contact (110) formed through an insulator (85) to electrically connect the gate stack (60) to an overlying metal line (100). The gate stacks have a polysilicon or silicide electrode. The metal can be a copper alloy (see column 4, lines 46-48). These are limitations set forth in claims 19, 22 of the applicant's invention.

However, Bronner et al. do not teach or suggest a gate electrode with rhodium, ruthenium, iridium, osmium or platinum as a main constituent (a limitation of claim 19), nor do they teach or suggest a multilayered gate electrode with a first conductive film that includes silicon and with a second conductive film, nearer to the plug, that includes rhodium, ruthenium, iridium, osmium or platinum as a main constituent (limitations of claim 22).

Psaras et al. teach a gate electrode comprising a lower layer of polysilicon (26) and an upper layer of Rh_2Si (i.e. an upper layer with rhodium as a main constituent) (see Fig. 5 and column 12, lines 9-47). Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Bronner et al. and Psaras et al. in order to use a polysilicon/ Rh_2Si gate electrode as taught by Psaras et al. Psaras et al. recognize that silicides like Rh_2Si can be used in gate electrodes for making ohmic contacts (see column 1, lines 20-22 and column 10, lines 32-42).

Allowable Subject Matter

4. Claims 14-15, 17-18, 20-21, 23-24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

- Claims 14-15 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a plug that comprises a main conductive film that includes copper as a main constituent element and an adjacent conductive film formed outside the main conductive film, wherein the adjacent conductive film includes rhodium, ruthenium, iridium, osmium, or platinum as a main constituent and palladium, cobalt, nickel, or titanium as an additional constituent;
- Claims 17-18 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a connection layer that comprises a main conductive film that includes copper as a main constituent element and an adjacent conductive film formed outside the main conductive film, wherein the adjacent conductive film includes rhodium,

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ruthenium, iridium, osmium, or platinum as a main constituent and palladium, cobalt, nickel, or titanium as an additional constituent;

- Claims 20-21 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a gate electrode that includes rhodium, ruthenium, iridium, osmium, or platinum as a main constituent and palladium, cobalt, nickel, or titanium as an additional constituent; and
- Claims 23-24 would be allowable because the prior art of record does not teach or suggest, in combination with the other claim limitations, a gate electrode that includes a first conductive film that includes silicon and a second conductive film that includes rhodium, ruthenium, iridium, osmium, or platinum as a main constituent and palladium, cobalt, nickel, or titanium as an additional constituent.

Response to Arguments

6. Applicant's arguments, see pages 4-8, filed 09 June 2004, with respect to the obviousness type double patenting rejection of claims 13-18 have been fully considered and are persuasive. This rejection of claims 13-18 has been withdrawn because claim 3 of US 6,624,513 in view of Bronner et al. (US 5,792,703) lacks at least the limitation of "an adjacent conductive film disposed outside of said main conductive film" as set forth in independent claims 13, 16 of the applicant's invention.

7. Applicant's arguments, see pages 8-11, filed 09 June 2004 with respect to the rejection of claims 13, 16, 19, 22 under 35 U.S.C. 103(a) have been fully considered but they are not persuasive.

Regarding the rejection of claims 13, 16 under 35 U.S.C. 103(a) as being unpatentable over Schacham-Diamand et al. (US 5,824,599) in view of Bronner et al. (US 5,792,703), the applicant argues that Schacham-Diamand et al. teach the dissolution of any platinum or rhodium that may be present in their catalytic seed layer (18). In fact, Schacham-Diamand et al. teach the dissolution of an overlying aluminum layer (19) as well as an alloy of the aluminum that forms with the catalytic seed material at the interface (18, 19) of the these layers. For the case of a copper catalytic seed layer, Schacham-Diamand et al. teach that a Cu-Al alloy is formed and subsequently dissolved in an electroless deposition bath, but Schacham-Diamand et al. recognize that some of the catalytic seed layer (18) must remain in order to function as a seed layer for a subsequent electroless copper deposition step (see column 6, lines 51-56 and column 7, lines 36-44). Further, Schacham-Diamand et al. disclose that either platinum or rhodium may alternatively be used as the catalytic seed layer (18), in which case a Pt-Al alloy or a Rh-Al alloy will be formed instead of the Cu-Al alloy and will be subsequently removed to expose the remainder of either the platinum catalytic seed layer (18) or the rhodium catalytic seed layer (18) (see column 7, lines 29-35). The use of either platinum (Pt) or rhodium (Rh) as an alternative catalytic seed material to copper (Cu) is more evident from the claimed invention of Schacham-Diamand et al., in

which they definitively claim "said catalytic seed layer is formed by depositing Ni, Co, Ag, Au, Pd, Pt, Rh, or Cu" (see column 11, lines 21-22, 48-49).

Regarding the rejection of claims 19, 22 under 35 U.S.C. 103(a) as being unpatentable over Bronner et al. (US 5,792,703) in view of Psaras et al. (US 4,803,539), the applicant argues that the combination of Bronner et al. and Psaras et al. lack a layer of rhodium, ruthenium, iridium, osmium, or platinum. However, claims 19, 22 do not claim such a layer. Instead, claims 19, 22 use open claim language (i.e. the term "includes") to limit the gate electrode material. Specifically, claim 19 (see lines 10-12) has the limitation "said gate electrode includes as a main constituent element at least one element selected from a group consisting of rhodium, ruthenium, iridium, osmium and platinum", while claim 22 (see lines 14-16) has the limitation "said second conductive film includes as a main constituent element at least one element selected from a group consisting of rhodium, ruthenium, iridium, osmium and platinum". The gate electrode taught by Psaras et al., which comprises a lower layer of polysilicon (26) and an upper layer of Rh₂Si (see Fig. 5 and column 12, lines 9-47), meets these limitations as currently set forth in claims 19, 22 of the applicant's invention, because their rhodium silicide layer has two parts rhodium to one part silicon and rhodium is therefore the main constituent of this upper layer.

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SWS

Stephen V. Smoot
Patent Examiner
Art Unit 2813